Performance Evaluation of Polymers for Bumping and Wafer Level Packaging

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Purpose

- Design a mask set to evaluate polymers in multilayer applications
  - Optimize polymer performance and reliability
  - Optimize metallization process
    - Polymer and metallization cannot be tested separately because of process interaction
- Obtain quantitative data
  - Design to use minimal instrumentation
  - Minimize testing time
  - Remove subjective evaluation factors
  - Separate performance evaluation from processing convenience
- Shorten overall polymer evaluation cycle
- Applicable to internal or out-sourcing evaluation

Uncover the processing boundaries of materials

- Push materials and processes to their limit
  - Photolithographic patterns designed to check the limits of materials
    - Inability to achieve perfect results with a mask set is not a failure
      - It allows to uncover weaknesses in materials and process
  - Too often test patterns are designed specifically for a product development and never find the real capabilities of materials
    - Conceals real capability of material
    - Hide potential failures modes
  - Incomplete testing cost money in the long run
    - Need to repeat tests for the next product development cycle because of lack of confidence if the materials will work or not
- Final test criteria need to be process independent

Electrical tests related to polymers

- Effective dielectric constant
  - Parallel plate capacitors
- Surface leakage
  - Triple tracks:
    - Ground lines parallel on each side of a conductor
- Effect of humidity on ε' and ε''
  - Meshed capacitors allowing faster sensitivity to water vapor diffusion
- Dielectric integrity
  - Verification of the lack of pinhole from one dielectric level to the next
- Transmission lines
  - Dielectric properties determine transmission lines geometries
  - T Lines include vias to test and model high speed performance

Tests related to metallization

- Metallization resistivity
  - Single level Van der Pauwn
  - Line width control structure
- Interlevel connections
  - Multi-level Van der Pauwn
  - Daisy chains for reliability
- Electrical
  - Long lines with Kelvin pads
  - Cross-talk (parallel lines)
  - Impedance (shorts and opens)
  - Capacitive structures
  - Measurements of metal and dielectric losses
  - Matching design criteria given by rf theory and measurements

Optimizing resolution of photosensitive materials

- A special pattern is used to monitor optimal exposure and development
  - Mask consist of squares with slowly increasing separation between them
- Optimum resolution is achieved when overlap between squares is minimum
  - Overlap very sensitive to photolitho processing parameters
    - focus, mask / wafer separation, development
- Performance evaluation accomplished with a simple visual inspection

Polymer thickness measurement

- Optical instrument best for measuring thick polymer layers
  - Stylus instruments:
    - Good for metals
    - Inoperative with wet films
- Spectroscopic reflectance
  - Newer instruments designed to work with thicker films
  - Thickness mapping instruments are inexpensive and quick
- Need to obtain the index of refraction data
  - n and k from UV to near IR
  - Can estimate n and k if not given by manufacturer
  - n and k may be different for wet and cured polymers
    - Solvent affects the complex index of refraction

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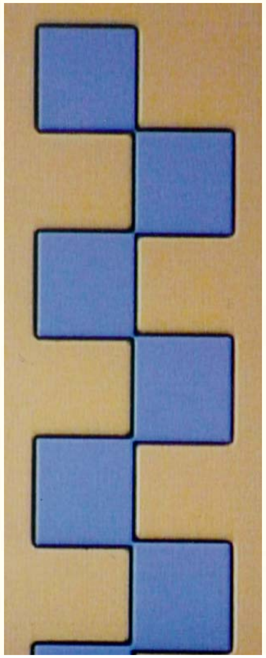
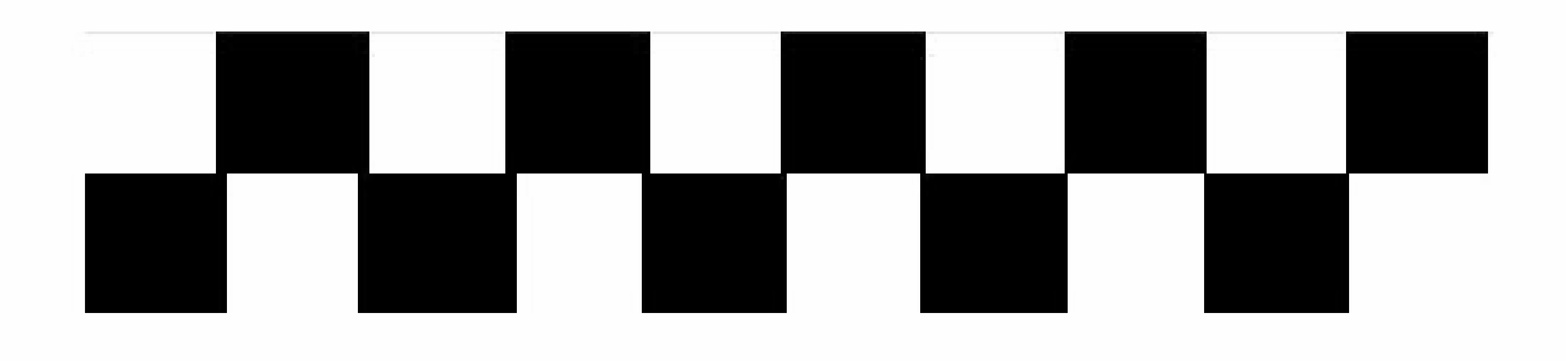
Optimal photolitho processing



- Processing positive acting material:
  - overexposure increase overlap
  - underexposure decrease overlap
- Negative acting material
  - overexposure decrease overlap
  - underexposure increase overlap



Pattern to evaluate photolitho resolution

- Useful with photosensitive materials or pattern etching
  - Equal space and linewidth elements (equispace on the mask)
    - Evaluate quantitatively the resolution following optimization of the exposure and development
  - Positive and negative elements present in the pattern
    - Simultaneous accurate reproduction of small dots and vias cannot be achieved
    - Allow to determine and measure best compromise
    - Optimization is a compromise between conflicting requirements
- Mask bias
  - determined from measurements of the pattern after photolitho

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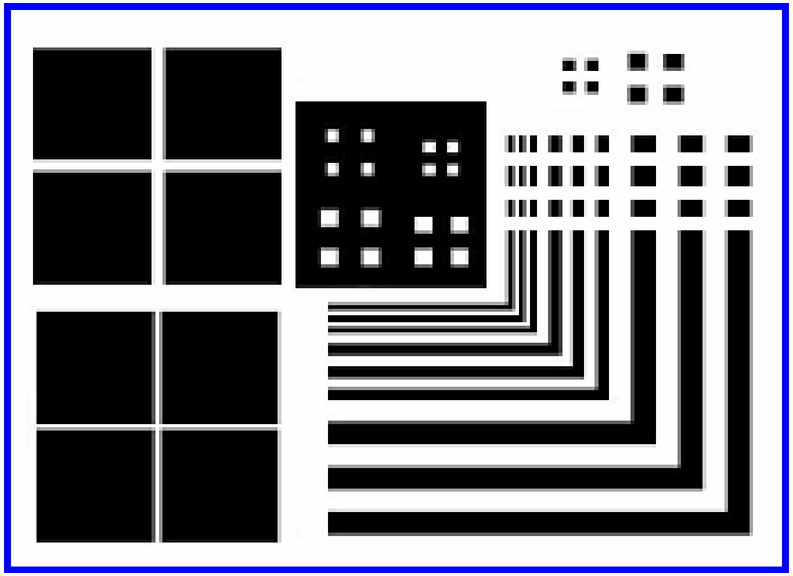
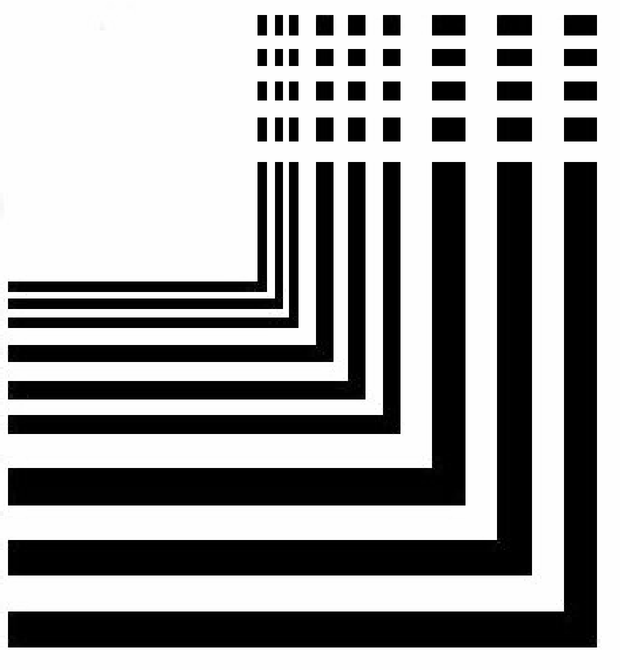
Resolution target

- Elements are large enough to be able to pass a stylus profilometer
- Parallel lines can be used to evaluate planarisation capabilities of the dielectric



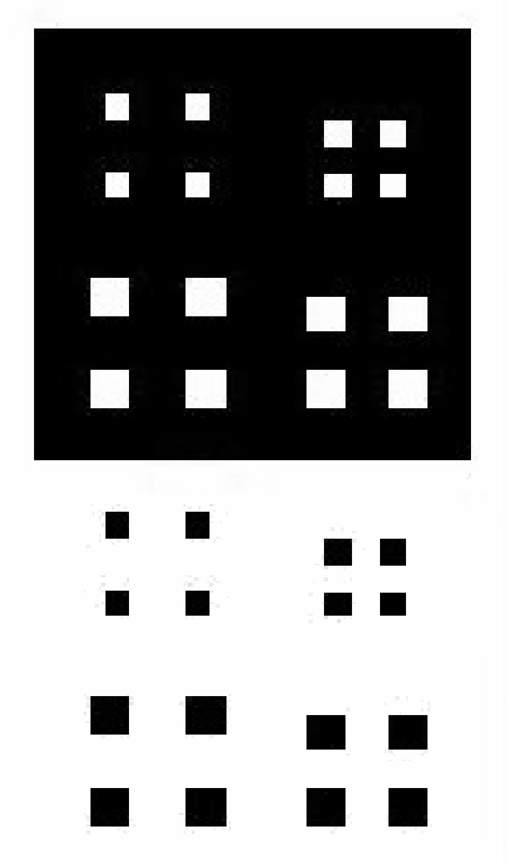
Equispaced lines

- Linewidth is incremented in steps
- Rounding of corners after processing
  - Mask acts as a spatial low pass filter
  - Check on focus or distortion caused by mask to wafer separation
- Reproduction fidelity
  - Optimize exposure, mask separation, focal point as needed for best preservation of line / space width
  - Very small and large geometries cannot be optimized simultaneously



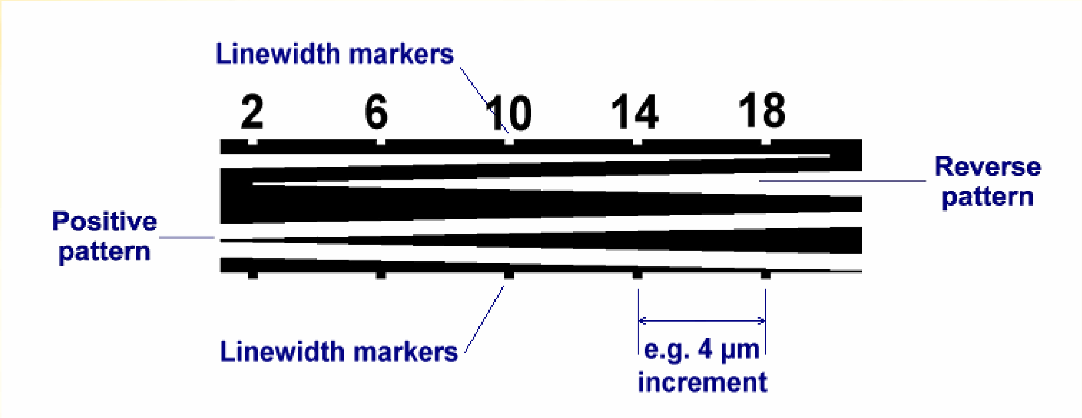
Negative and positive elements

- Small blocks and small vias
  - Difficult to optimize simultaneously
  - Rounding of corners becomes obvious
- Optimize
  - compromise between mask separation or projection focal point
  - Development
    - Concentration
    - Agitation
  - Wet etchant
    - Reveals gas trapping problem
      - Most often hydrogen, e.g. Al etch
    - Wetting properties, agitation



Minimum resolvable linewidth

- Works equally well for positive or negative materials
- Tip of pointed lines disappear with loss of resolution
- Resolution readily determined by inspection



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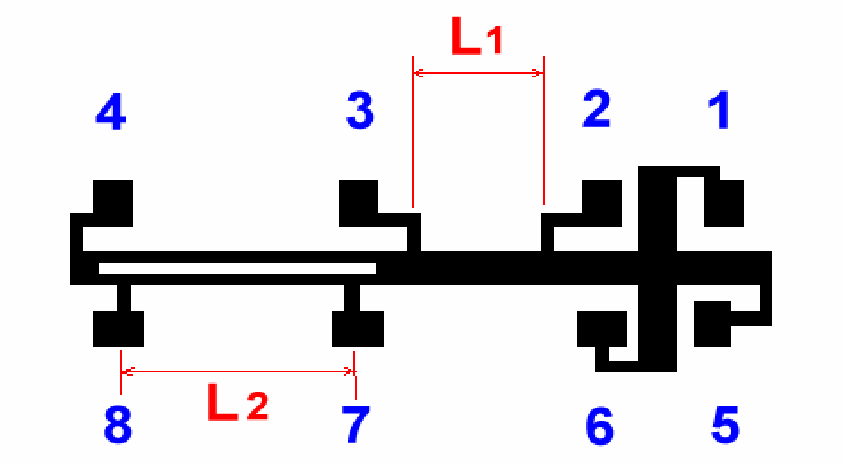
Electrical measurement of linewidth & space (metals)

- Van der Pauw cross: measures sheet resistivity $R_s = \left(\pi / \ln 2\right)\left(V_{3-4} / I_{5-6}\right)$
- Straight conductor: linewidth $W_{2-3} = 2W + S = R_s L_1 \left(I_{1-5} / V_{2-3}\right)$
- Split conductor:
  - Linewidth $W_{7-8} = 2W = R_s L_2 \left(I_{1-5} / V_{7-8}\right)$
  - Space $S = W_{2-3} - W_{7-8}$



Pattern developed by Jet Prop. Labs
NASA Tech Brief July 1987
Vol 11, #7 item 68

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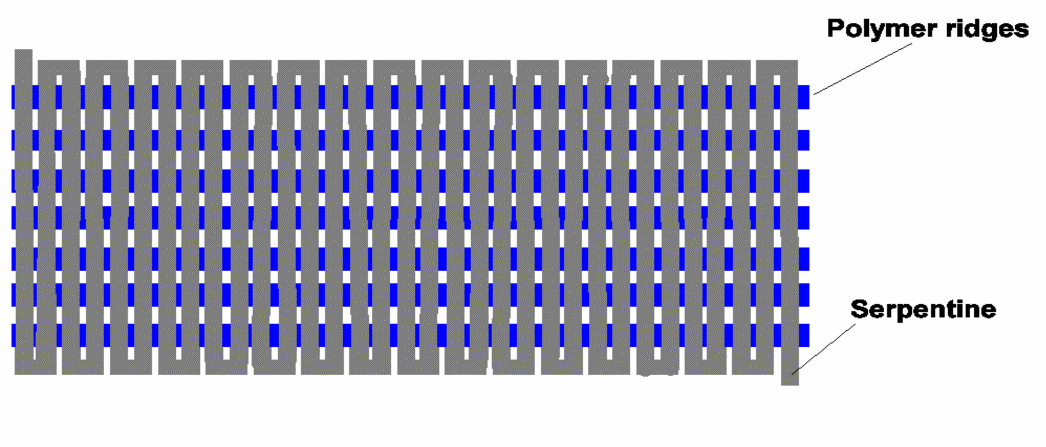
Step coverage

- Serpentine line
  - Long conductors over topography
    - Equispaced polymer lines to create topography
    - Variations in topography line spacing reveals sensitivity of step coverage to topography
  - Long serpentine line with no topography used as reference
- Measure serpentine line resistivity
  - Resistivity tracks thickness and linewidth variations
    - Thinning of metallization lines over steps
    - Narrowing of lines due to photolitho over different planes
    - Cracking from thermal excursions
- Record percent increase in resistivity: line over topography versus line on flat surface for each step height

Serpentine for step coverage

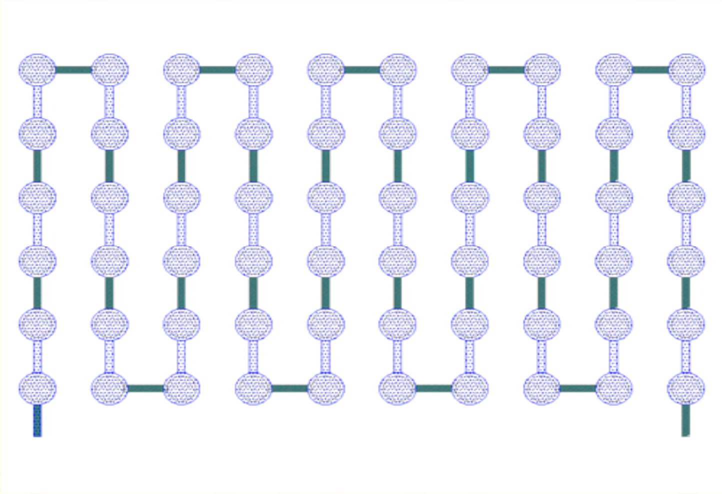
- Cause of linewidth variations in serpentine over topography:
  - Differential in mask to metal separation between top and bottom of the ridges (aligner)
  - Fixed focal point and short depth of focus (inherent to physics of stepper)



Daisy chains

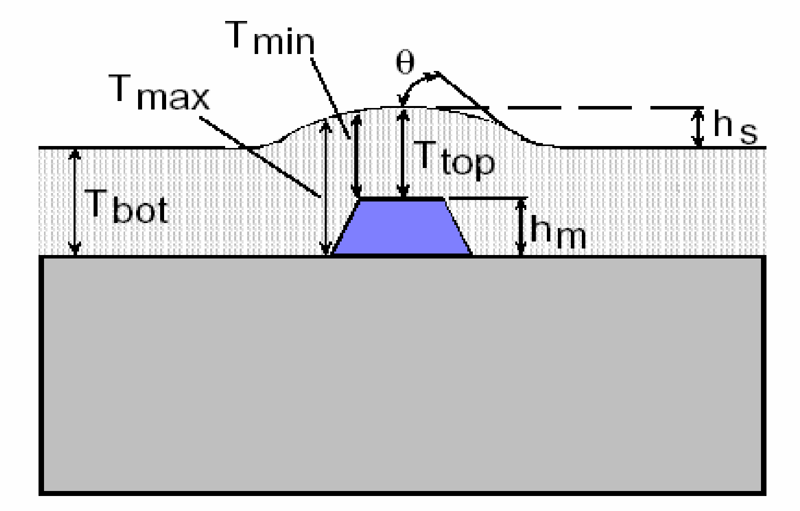
- Test vias between two or more metallization levels
- Test sensitivity of process to random faults in via contacts
- Should have probing pads at regular intervals to allow isolation of faults location
- Can include Van der Pauw pad structures to verify single via resistivity if needed

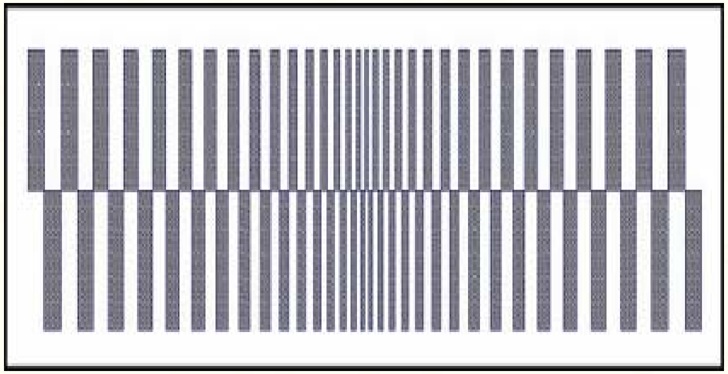
L.J. Van der Pauw, Philips Technical Review, vol. 26, #8, p. 220 (1958)



Planarization

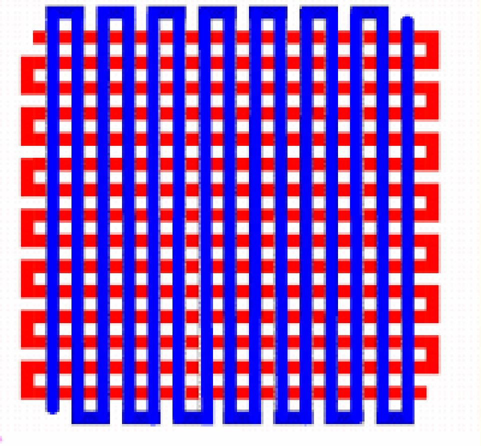
- Degree of planarization
  - DOP = 1 - h_s/h_m
  - Thickness dependant
  - Linewidth and space dependant
- Need pattern with variable linewidth / space grating





Random defect test pattern

- Test dielectric integrity
  - Pin holes detection
  - Serpentine line over solid metal plane
- Test for faults in metal lines
  - Use two orthogonal serpentine metallization
  - Test for shorts
    - Between top and bottom metallization levels
    - Between lines in a loop
  - Breaks in lines



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Capacitors

- Area capacitance
  - Parallel plate caps
  - Need accurate thickness of polymer and metals
- Fringe capacitance
  - Comb capacitors
  - Can be used to measure surface leakage
- Cross-over capacitor
  - Line to line capacitance coupling at cross-overs

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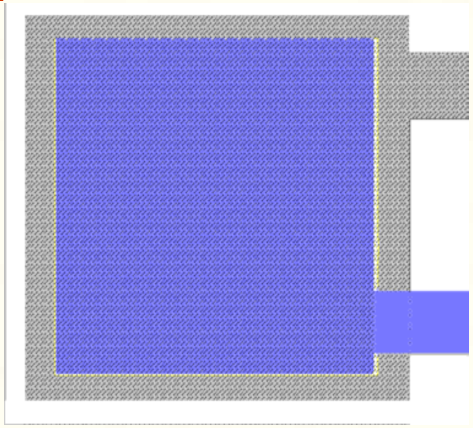
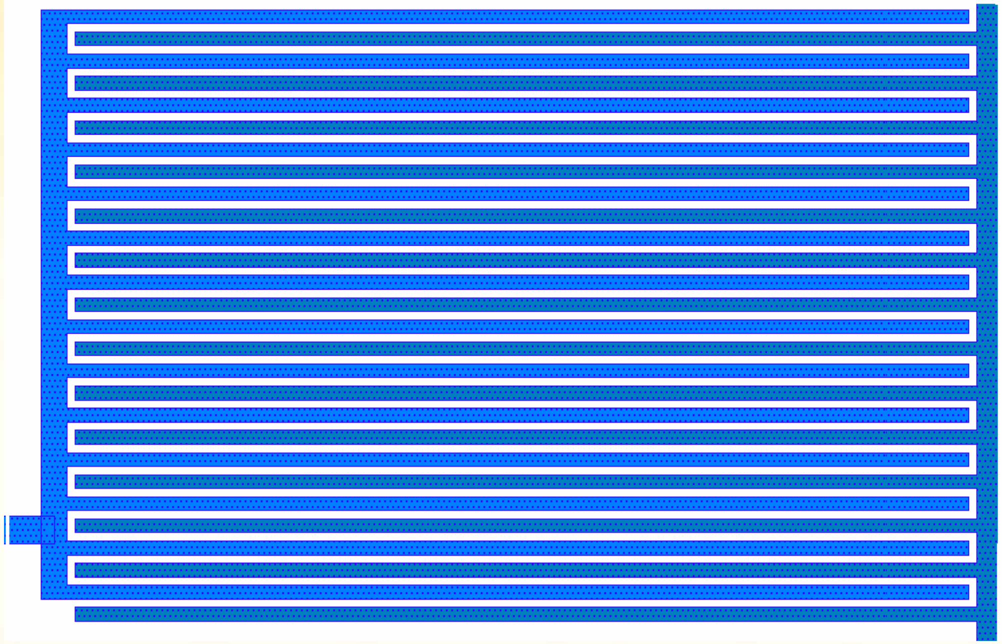
Parallel plate capacitor

- $C = \varepsilon\varepsilon_o A/D$
  - Where: ε = Relative Dielectric
  - Constant of Insulator
  - ε_o = 8.854e-14 F/cm
  - A = Area of Electrodes (cm2)
  - D = Distance between
  - Electrodes (cm)
- Measured value includes fringing capacitance (neglected above



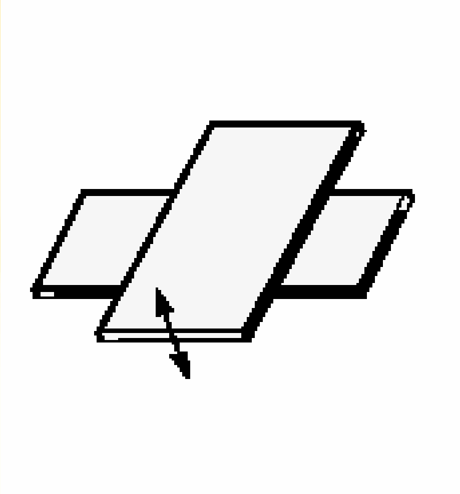
Comb capacitor

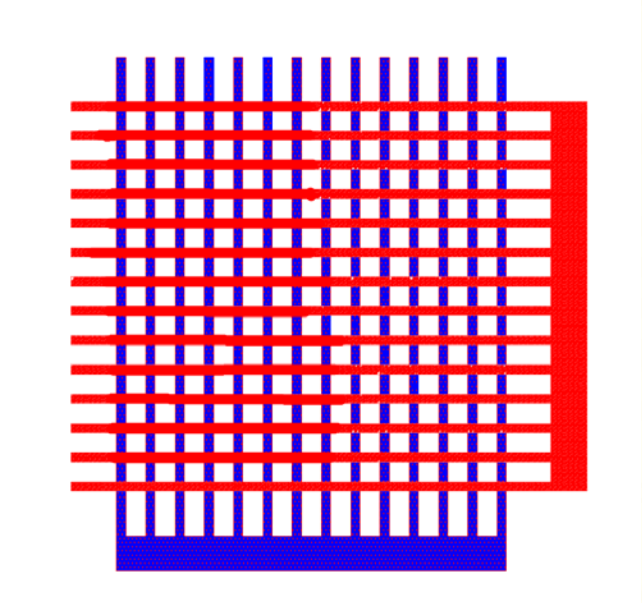
- Moisture sensitive
  - Basis for hygrometer
  - Reveal moisture sensitivity
- Capacitor design ref.: J.C. Hurt, C.L. Mohr, “A CAD design system for Hybrid circuits” IEEE CHMT-3, 525 (1980)



Cross-over capacitor

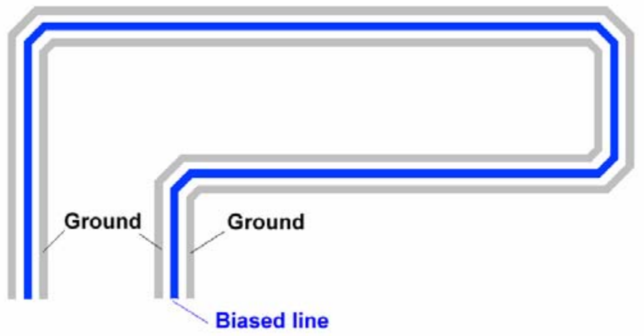
- Characterize cross-over parasitic capacitance between conductor lines
- Basically a parallel plate capacitor
  - Fringe capacitance large relative to size





Triple track

- Test surface leakage of dielectric
  - Biased line surrounded by grounded lines exposed to temperature and humidity (usually 85 RH - 85 ºC)
  - Measure conductivity between line and ground
  - Measure resistivity change of conductors
- Sensitive to surface contamination
  - Water absorption in polymer
  - Ionic migration of metallization
  - Corrosion



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Conclusion

- Specialized test patterns for polymer performance evaluation do:
  - Saves testing time
  - Reduces development and later manufacturing control costs
  - Allow optimization of processes with minimum efforts
  - Find the boundaries of processes
  - Provides information not available from a working device mask set
  - Provides real time monitoring of process and direct visual feedback
  - Leads to solid design rules based on statistical data
  - Gives realistic direct comparison of materials
    - Independent of process details
    - Evaluation done strictly on measurements

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