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High Density Multichip Modules for the Circuit Designer

by

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HIGH DENSITY MULTICHIP MODULES FOR THE DESIGNER

INTRODUCTION

- BACKGROUND
- EVOLUTION OF ELECTRONIC PACKAGING
- PURPOSE OF HIGH DENSITY MULTICHIP MODULES

CHOSING THE RIGHT TECHNOLOGY

- HIGH DENSITY MULTILAYER TECHNOLOGY
  - POLYMER - VACUUM DEPOSITED METALLIZATION
  - POLYMER - ELECTROLYTIC METALLIZATION
  - INORGANIC DIELECTRICS
- SILICON PROGRAMMABLE CIRCUIT BOARDS
- ULTRA FINE LINES PRINTED CIRCUIT BOARDS
  - PREPREG LAMINATES
  - CAST POLYMERS
- CONVENTIONAL HYBRID TECHNOLOGIES
  - MULTILAYER THICK FILM CIRCUITS
  - MULTILAYER THIN FILM CIRCUITS
  - MULTILAYER COFIRED CERAMIC
    - CONVENTIONAL PROCESS
    - LOW TEMPERATURE COFIRED CERAMIC

BENEFITS OF THIN-FILM/POLYMER APPROACH

- ELECTRICAL PERFORMANCE
  - BENEFITS OF SHORT INTERCONNECTIONS
  - IMPEDANCE CONTROL
  - MINIMIZATION OF TIME DELAYS
- MECHANICAL
  - WEIGHT REDUCTION
  - VOLUME REDUCTION
  - AUTOMATIC ASSEMBLY
- RELIABILITY
  - RESISTANCE TO THERMAL SHOCKS
  - RESISTANCE TO VIBRATIONS
  - SYSTEM RELIABILITY
- THERMAL
  - REDUCTION OF POWER DISSIPATION
  - HIGH THERMAL CONDUCTIVITY SUBSTRATES
  - DIRECT HEAT REMOVAL

DESIGN METHODOLOGY

- IMPLEMENTING THE CORRECT TYPE OF CIRCUITS
  - DIGITAL
    - CMOS
    - ECL
    - GaAs
    - OTHERS
  - ANALOG
  - TYPE OF APPLICATION
    - PHYSICAL SIZE AND WEIGHT
    - SPEED / PERFORMANCE ORIENTED
    - HIGH RELIABILITY
- CIRCUIT PARTITIONING
  - SYSTEM COMPLEXITY
  - LEVEL OF SILICON INTEGRATION
  - PACKAGE AVAILABILITY
  - PIN-OUT CONSTRAINTS
  - MCM SUB-CARRIER BOARD
- ELECTRICAL PERFORMANCE
  - IMPEDANCE CONTROL
    - GEOMETRIC EFFECTS
    - DIELECTRIC EFFECTS
    - MEASURED VALUES IN HDMI STRUCTURES
  - TIME DELAYS
    - RESISTANCE
    - CAPACITANCE
    - INDUCTANCE
    - PERFORMANCE MODELLING
    - MEASUREMENTS
- THERMAL MANAGEMENT REQUIREMENTS
  - THERMAL BALANCE IN HDMI
    - REDUCTION IN OVERALL POWER REQUIREMENTS
    - AERAL POWER DENSITY INCREASE
  - THERMAL OPTIONS
    - SUBSTRATES
      - Silicon
      - Aluminum Nitride
      - Silicon Carbide
      - Alumina, Diamond, Others
    - DIELECTRICS THERMAL PROPERTIES
      - Polymers
      - Inorganic Dielectrics
    - SEMICONDUCTOR DIES MOUNTING
      - UNDER THE CHIPS ROUTING
        - Chips on top of the polymer
        - Thermal Vias
      - BLOCK ROUTING (AROUND THE CHIPS)
        - Chips in contact with the HDMI substrate
        - Chips recessed in cavities
- INTERCONNECTION LAYOUT TRADE-OFFS
  - THEORETICAL WIRING CAPACITY
  - WIRING CAPACITY IN REAL DESIGNS
  - EXAMPLES OF REAL DESIGNS

INTERCONNECT LAYOUT DESIGN

- CRITERIA FOR SUBSTRATE DIMENSIONS
  - MAXIMUM SUBSTRATE SHAPE AND SIZE
  - USEABLE AREA
  - REQUIREMENTS FOR REGISTRATION MARKS
    - SPECIAL REQUIREMENTS
- I/O PLACEMENT
  - MECHANICAL DATA ON CHIPS
  - CHIP PLACEMENT CONSTRAINTS
  - MULTICHIP MODULE I/O LOCATION
  - DECOUPLING CAPACITORS REQUIREMENTS
  - RESISTORS PLACEMENT
- FLOOR PLANNING
- CONDUCTOR LAYOUT REQUIREMENTS
  - CONDUCTOR WIDTH
  - CONDUCTOR SPACING
  - TRACE BENDING
    - 45 DEGREES, 90 DEGREES
  - CONDUCTOR PROTECTION
  - AUTOMATIC ROUTERS
  - ELECTRICAL SIMULATION
- VIAS CONSIDERATIONS
  - VIA PHYSICAL SIZE
  - VIA ELECTRICAL CHARACTERISTICS
  - TYPE OF VIAS
    - STAGGERED
    - STAIRCASE
    - FOLDED STAIRCASE
    - PLUGGED
  - NUMBER OF VIAS AND LOCATION
    - LIMITING THE NUMBER OF VIAS PER NETWORK
    - VIAS PLACEMENT ON THE SUBSTRATE
- POWER AND GROUND PLANES
  - SOLID PLANES
  - GRIDDED PLANES
- RESISTORS
  - DISCRETE CHIPS
  - INTEGRATED RESISTORS
    - DESIGN
    - TESTING AND TRIMMING
- CAPACITORS
  - DECOUPLING CAPACITORS
  - INTEGRATED CAPACITORS
- DESIGN OF DIE SITES
  - FOOTPRINT
  - GUARD BAND FOR ASSEMBLY
- DESIGN OF BONDING PADS
  - PADS ON TOP OF THE POLYMER
  - PADS AT THE SUBSTRATE LEVEL
  - PADS LOCATION AROUND DIES
- CHIP BONDING PADS METALLURGY
  - ALUMINUM, GOLD, SOLDERABLE

TESTING IN MCM's

- TYPES OF SUBSTRATE TESTERS
  - RESISTIVE
  - CAPACITIVE
  - COMPUTER OPTICAL INSPECTION
  - SEM VOLTAGE CONTRAST
- SYSTEM LEVEL TESTING
- RELIABILITY TESTING
  - SUBSTRATE
  - SYSTEM
  - COMPLETED MCM

ASSEMBLY PROCESS

- SEMICONDUCTOR DIE MOUNTING
  - FOOTPRINT
- DISCRETE PASSIVE COMPONENTS MOUNTING
- COMPONENTS INTERCONNECTION
  - CHIP AND WIRE
    - WIRE BOND PLACEMENT
    - THERMO-SONIC BONDING
    - ULTRASONIC WEDGE BONDING
      - GOLD
      - ALUMINUM
    - RIBBON BONDING
  - TAB
    - SINGLE-POINT THERMO-SONIC
    - WOBBLE-ATTACH
    - THERMAL SOLDER REFLOW
    - LASER BONDING
  - FLIP-CHIP
    - C4 PROCESS
    - INDIUM SOLDER BALLS
    - COINED GOLD BALLS
  - WHICH CHIP ATTACH TECHNIQUE ?

PACKAGING DESIGN

- LARGE KOVAR PACKAGES
- COFIRED ALUMINA PACKAGES
- COFIRED ALUMINUM NITRIDE PACKAGES
- CURRENT PACKAGE AVAILABILITY
- FUTURE AVAILABILITY

ECONOMICS OF HDMI

- YIELDS AND COST
- LINEWIDTH AND TOTAL SIZE TRADE-OFFS
- ELIMINATION OF INTERMEDIATE PACKAGES
- CURRENT DEVELOPMENT COSTS
  - NON-RECURRING COSTS
    - DESIGN COSTS
      - DIRECT COST
        - COMPUTER SIMULATIONS
          - THERMAL
          - ELECTRICAL
          - MECHANICAL
          - ASSEMBLY
          - TESTING
        - DESIGNER'S TIME AND TOOLS
        - DATABASE PREPARATION FOR TESTING
      - INDIRECT
        - OVERALL SYSTEM DESIGN
        - IN-HOUSE DATA GATHERING
        - DOCUMENTATION PREPARATION FOR VENDOR
    - TOOLING COSTS
      - MASK MAKING
      - PROGRAMMING OF TEST EQUIPMENT
  - PARTS COST
    - CURRENT
    - PROJECTED
  - FUTURE DEVELOPMENT COSTS
    - NON-RECURING
      - EVOLUTION OF DESIGN TOOLS
        - ROUTING
        - SIMULATION
          - ELECTRICAL
          - THERMAL
          - MECHANICAL
        - TESTING DESIGN
      - EVOLUTION OF TOOLING PREPARATION EQUIPMENT
      - EVOLUTION OF DESIGN METHODOLOGY
    - PARTS COST
      - INFLUENCE OF PHYSICAL SIZE ON COST
      - TRENDS IN SEMICONDUCTOR COSTS

CONCLUSION